UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/632,652 | 08/02/2003 | Arne W. Ballantine | END9-2000-0086-US2 | 3570 |

30449 7590 08/09/2005

SCHMEISER, OLSEN + WATTS
3 LEAR JET LANE
SUITE 201
LATHAM, NY 12110

| EXAMINER | |
|---|---|
| TSAI, H JEY | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2812 | |

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/632,652 | BALLANTINE ET AL. | |
| | Examiner | Art Unit | |
| | H.Jey Tsai | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-43 and 45-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43 and 45-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-17, 19, 21-24, 26-28, 30-38, 40-43, 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over LaFollette et al. 6,610,440, previously cited, in view of Jenson 6,924,164, newly cited.

The reference(s) teach the features :

LaFollette et al. discloses a method for forming an electrochemical structure within an integrated circuit comprising the step of:

providing a semiconductor wafer, col. 18, lines 30+,

forming a layer 30 of electronic devices (inherently a part of integrated circuit, IC, col. 12, lines 41-65) on the semiconductor wafer, wherein the layer of electronic devices includes at least one electronic device, fig. 3+ and col. 20, lines 15+,

forming N wiring levels within an interconnect structure of the integrated circuit-wherein the N wiring levels are disposed on the layer of electronic devices, wherein N is at least 1, wherein the N wiring levels are denoted as wiring level 1, wiring level 2 , ....., fig. 3+,,

forming a first conductive metalization 46 and a second conductive metalization 47 (or 49) within the N wiring levels,

forming at least one battery 44' within the wiring levels (1 and 2, first and second level or ribbon connection in fig. 3 can be replaced with thin film interconnect, see col. 25, lines 20+, that is I=1 through K....., wherein I is selected from the group consisting of 1, 2, ....N, wherein K is selected from the group consisting of I, I+1,.... and N), wherein the first conductive metalization 46 conductively couples a first electrode 34" of the at lest one battery 44' to the at least one electronic device 59, 59', wherein the second conductive 47 representation conductively couples a second electrode 40" of the battery to the at least one electronic device, and wherein the first and second conductive metalization are totally external to the interior of the at least one battery, fig. 4+, col. 25, lines 55+,

forming a trench (cavity) 42' within ILD layer 38", col. 23, lines 1+,

depositing electrolyte layer,

forming first and second battery electrode (anode and cathode) with Zn, col. 13, lines 38+.

Jenson et al. discloses a method for forming an electrochemical structure within an integrated circuit comprising the step of:

providing a semiconductor wafer 55, col. 8, lines 65-67, fig. 1D,

forming a layer 2510 of electronic devices on the semiconductor wafer, wherein the layer of electronic devices includes at least one electronic device, fig. 25 and col. 44, lines 15-32,

forming N wiring levels within an interconnect structure of the integrated circuit-wherein the N wiring levels are disposed on the layer of electronic devices, wherein N is at least 2, wherein the N wiring levels are denoted as wiring level 1...2, fig. 1D,

forming a first conductive metalization 57 and a second conductive metalization 65 within the N wiring levels,

forming at least one battery 59/61/63 within the wiring levels, wherein the first conductive metalization 57 conductively couples a first electrode 61 of the at lest one battery 59/61/63 to the at least one electronic device 2510, wherein the second conductive 65 representation conductively couples a second electrode 63 of the battery to the at least one electronic device, and wherein the first and second conductive metalization are totally external to the interior of the at least one battery,

The difference between the reference(s) and the claims are as follows: LaFollette et al. teaches forming a battery within conductive layer but does not teach more conductive layers formed over the battery. However, Jenson et al. teaches at fig. 1D, there are more conductive layers 65....77 formed over battery 59/61/63.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Lafollette et al.'s process by forming more conductive layers as suggested by Jenson because more batteries can be formed within all the conductive layers.

Claims 18, 20, 25, 29, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over LaFollette et al. 6,610,440 in view of Jenson, as applied to claims 15-17,19, 21-24, 26-28, 30-38, 40-43, 45-48 above, and further in view of Bates et al. 5,561,004 and Wolk et al. 2001/0000744, previously applied.

LaFollete et al. teaches forming an electrochemical structure of battery within an integrated circuit but does not teach using lithium phosphorous oxynitride as an

electrolyte. However, Bates et al. teaches at col. 2, lines 15-25, using lithium phosphorous oxynitride as an electrolyte 26 for a battery and Wolk et al. teaches at para. 35 and 90, using a diffusion battery layer for a battery.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified above reference by using lithium phosphorous oxynitride and forming a diffusion barrier layer as suggested by Bates and Wolk et al. because lithium phosphorous oxynitride can be formed as a layer structure on the cathode that is compatible with the semiconductor process and forming a diffusion layer to prevent corrosion formed on the cathode electrode.

Applicant's arguments filed June 15 have been fully considered but they are not persuasive. Because LaFllette clearly teaches at fig. 9 and col. 20, lines 15-25, battery 82 is formed over the microcircuit 80 on the same the substrate/device by using IC fabrication techniques. And, there is not seen in the claim 15, that there is an existence of at least one more wiring layer formed above the battery. Claim 15 merely claimed I is selected from the group consisting of 1, ...N and K is selected from the group consisting of I.....N-1, therefore, when N is equal to 2, then K is equal 1. LaFollette clearly teaches at fig. 3, the second electrode layer 40" (N=2) of battery is the last layer of wiring layer and first electrode layer 34" (K=1) of battery is the second to the last wiring layer. Newly cited reference, Jenson teaches forming more conductive layers over the battery in fig. 1D and forming a battery 2320 over an electrode device 2510 in fig. 1D as set forth above.

Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the Group customer service whose telephone number is (703) 308-4357.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebenttric can be reached on (571) 272-1873.

The fax phone number for this Group is 571-273-8300.

hjt

8/7/2005

H. Jey Tsai
Primary Examiner
Patent Examining Group 2800